CLAIMS

1. A memory device comprising a memory cell formed over an insulating surface, which includes a semiconductor film having two impurity regions, a gate electrode, and two wirings connected to the respective impurity regions,

wherein the semiconductor film interposed between the two wirings of the memory cell is altered by applying a voltage between the gate electrode and at least one of the two wirings.

2. The memory device according to claim 1, wherein the memory device comprises two or more gate electrodes.

3. The memory device according to claim 1, wherein the semiconductor film is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings.

4. A memory device comprising a first memory cell and a second memory cell formed over an insulating surface, each of which includes a semiconductor film having two impurity regions, a gate electrode, and two wirings connected to the respective impurity regions,

wherein the first memory cell comprises an initial state; and

the semiconductor film interposed between the two wirings of the second memory cell is altered by applying a voltage between the gate electrode and at least one of the two wirings.

5. The memory device according to claim 4, wherein the memory device comprises two or more gate electrodes.

6. The memory device according to claim 4, wherein the semiconductor film is altered to an insulating state by applying a voltage between the gate electrode

and at least one of the two wirings.

7. A memory device comprising a memory cell formed over an insulating surface, which includes a semiconductor film having one or two impurity regions, an electrode, and two wirings connected to the respective impurity regions,

wherein the semiconductor film interposed between the two wirings of the memory cell is altered by applying a voltage between the electrode and at least one of the two wirings.

8. The memory device according to claim 7, wherein the electrode is interposed between the two wirings.

9. The memory device according to claim 7, wherein the memory device comprises two or more electrodes.

10. The memory device according to claim 7, wherein the semiconductor film is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings.

11. A memory device comprising a first memory cell and a second memory cell formed over an insulating surface, each of which includes a semiconductor film having one or two impurity regions, an electrode, and two wirings connected to the respective impurity regions,

wherein the first memory cell has an initial state; and

the semiconductor film interposed between the two wirings of the second memory cell is altered by applying a voltage between the electrode and at least one of the two wirings.

12. The memory device according to claim 11, wherein the electrode is interposed between the two wirings.

13. The memory device according to claim 11, wherein the memory device comprises two or more electrodes.

14. The memory device according to claim 11, wherein the semiconductor film is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings.

15. A manufacturing method of a memory device, comprising the steps of:

forming an island shape semiconductor film over an insulating surface;

forming a gate insulating film over the island shape semiconductor film;

forming a gate electrode over the gate insulating film;

doping an N-type impurity element with the gate electrode used as a mask, thereby forming an N-type high concentration impurity region in the island shape semiconductor film;

forming an interlayer film over the gate insulating film and the gate electrode;

forming a contact hole in the interlayer film and a wiring connected to the high concentration impurity region, thereby forming a memory cell, and

applying a voltage between the gate electrode and the wiring of the memory cell, thereby altering a channel region of the island shape semiconductor film to an insulating state.

16. The method of a memory device according to claim 15, wherein the memory device comprises two or more gate electrodes.